Through Thick and Thin: Tuning the Threshold Voltage in Organic Field-Effect Transistors

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CONSPECTUS: Organic semiconductors (OSCs) constitute a class of organic materials containing densely packed, over-lapping conjugated molecular moieties that enable charge carrier transport. Their unique optical, electrical, and magnetic properties have been investigated for use in next-generation electronic devices, from roll-up displays and radiofrequency identification (RFID) to biological sensors. The organic field-effect transistor (OFET) is the key active element for many of these applications, but the high values, poor definition, and long-term instability of the threshold voltage (V_T) in OFETs remain barriers to realization of their full potential because the power and control circuitry necessary to compensate for overvoltages and drifting set points decrease OFET practicality.

The drifting phenomenon has been widely observed and generally termed "bias stress." Research on the mechanisms responsible for this poor V_T control has revealed a strong dependence on the physical order and chemical makeup of the interfaces between OSCs and adjacent materials in the OFET architecture.

In this Account, we review the state of the art for tuning OFET performance via chemical designs and physical processes that manipulate V_T. This parameter gets to the heart of OFET operation, as it determines the voltage regimes where OFETs are either ON or OFF, the basis for the logical function of the devices. One obvious way to decrease the magnitude and variability of V_T is to work with thinner and higher permittivity gate dielectrics. From the perspective of interfacial engineering, we evaluate various methods that we and others have developed, from electrostatic poling of gate dielectrics to molecular design of substituted alkyl chains. Corona charging of dielectric surfaces, a method for charging the surface of an insulating material using a constant high-voltage field, is a brute force means of shifting the effective gate voltage applied to a gate dielectric. A gentler and more direct method is to apply surface voltage to dielectric interfaces by direct contact or postprocess biasing; these methods could also be adapted for high throughput printing sequences. Dielectric hydrophobicity is an important chemical property determining the stability of the surface charges. Functional organic monolayers applied to dielectrics, using the surface attachment chemistry made available from "self-assembled" monolayer chemistry, provide local electric fields without any biasing process at all. To the extent that the monolayer molecules can be printed, these are also suitable for high throughput processes. Finally, we briefly consider V_T control in the context of device integration and reliability, such as the role of contact resistance in affecting this parameter.
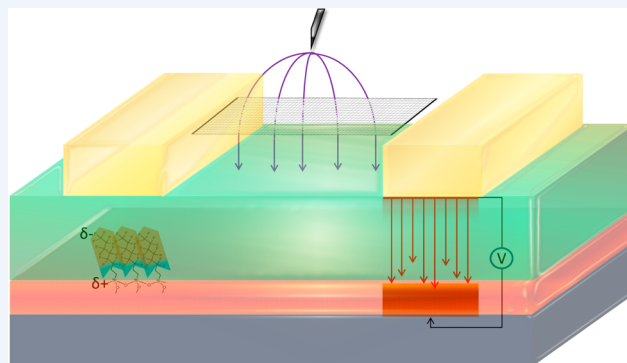
INTRODUCTION

Organic semiconductors (OSCs) have been the subject of intense research for their combination of optical, electrical, and magnetic properties. Conjugated moieties in close contact enable the overlap of molecular orbitals, facilitating carrier transport in OSC films consisting of small molecules and/or polymers. From a fabrication standpoint, their solubility in a wide spectrum of solvents and low sublimation and melting temperatures make them an attractive addition to the materials palette and ideal candidates for low-cost electronic devices. Organic field-effect transistors (OFETs) figure prominently in OSC research as the potential basis of digital logic for all-organic electronic systems. The requirements for OFETs in appropriate applications are similar to those of inorganic complementary metal-oxide-semiconductor (CMOS) transistors: low and stable operation voltage, high ON−OFF ratio, fast switching, and minimal OFF-current leakage.

Low-voltage operation is critical for most conceivable applications of organic electronics, namely, radio frequency identification (RFID), mobile displays, and implantable medical devices. In the digital sense, the operation of a transistor consists of switching from a logical 0 (OFF) to a logical 1 (ON). The current flowing in the ON state is given by the saturation regime approximation[1] as

$$I_D = (W/2L)\,\mu C_i (V_G - V_T)^2 \qquad (1)$$

Here the current I_D is the current flowing between the source and drain terminals; W and L are geometric terms for the electrode extent and separation, respectively; μ is the majority charge carrier mobility; C_i is the capacitance per unit area of the
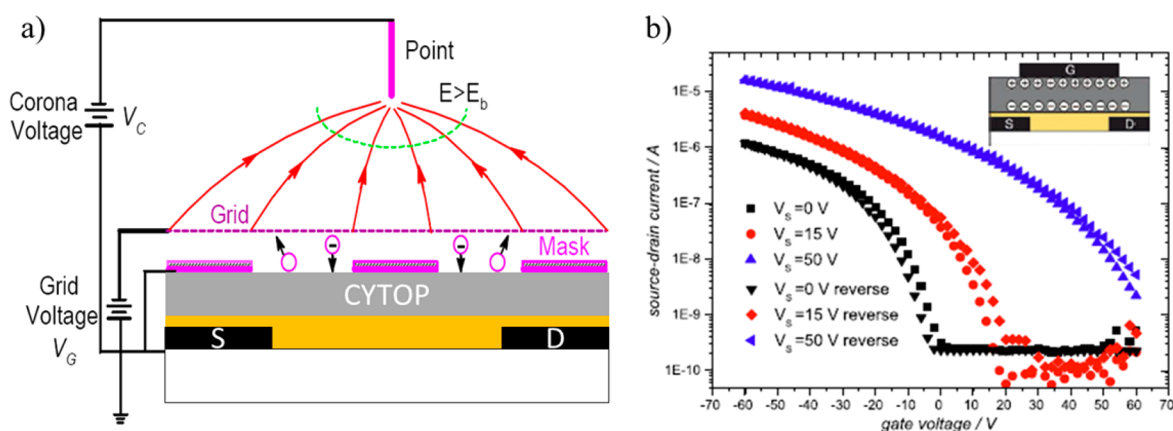
Figure 1. (a) Illustration of triode-corona charging of an organic dielectric. The corona voltage V_C between the top and bottom electrodes (as high as -8 kV), and the grid voltage V_G between the grid and bottom electrode (20−60 V), satisfy the relation $V_C \gg V_G$. Adapted image reprinted with permission from ref 19. Copyright Wiley. (b) Transfer curves for pristine and corona-charged OFETs, where V_S indicates the measured surface potential of the CYTOP layer. Devices were measured at $V_{DS} = -10$ V, and device $W/L = 500$. V_T was tunable from -5 V to $+37$ V. Image reprinted with permission from ref 15. Copyright Elsevier.

dielectric, given as $C_i = \varepsilon_i \varepsilon_0 / t_i$, where ε_i is the relative dielectric constant of the gate dielectric, ε_0 is the permittivity of free space, and t_i is the thickness of the dielectric; V_G is the voltage applied to the gate electrode, and V_T is the threshold voltage at which the transistor turns ON. Low-voltage organic circuitry relies on OFETs that exhibit considerably larger drain current in the ON state relative to their OFF state, with application of a minimal gate voltage. Initial approaches to increasing I_D have focused on reducing the transistor channel length, increasing the capacitance of the gate dielectric, and developing high-mobility OSCs.

In addition to low voltage operation, the control and stability of the V_T are critical for proper device operation. For an n-type (p-type) transistor, the ON state is maintained by keeping the Source electrode at ground, and the Gate and Drain at a high positive (negative) voltage. In this state, the dielectric is subjected to a high static electric field across its thickness. Maintaining the transistor in this state for extended periods of time results in a gradual shifting of the V_T toward higher accumulation voltages, requiring greater $|V_G|$ to achieve the same I_D. This V_T shift in a digital circuit ultimately leads to circuit failure, as the transistor requires more voltage to switch than its driving transistor can provide. This phenomenon has been termed "gate bias stress," and is associated with the buildup of charge and/or creation of dipoles at the OSC−dielectric interface,[2,3] capturing majority carriers in the OFET channel that would otherwise contribute to the net I_D. In this Account, we explore various physical and chemical methods that enable control over the value and stability of the V_T by modifying the OSC-dielectric interface.

One of the materials challenges associated with fabricating all-organic OFETs has been the development of high dielectric constant insulators.[4] Work by Acton et al.[5] employed an HfO$_2$ sol−gel dielectric ($\varepsilon \sim 16$−25), and our own group has developed a sol−gel sodium beta-alumina-like dielectric[6] with $\varepsilon \sim 170$. However, most organic insulators have relatively low dielectric constants ($\varepsilon \sim 2$−3), requiring V_G as high as $|100 \text{ V}|$ to turn on an OFET on a 100 nm thick dielectric, with a significant fraction of this potential constituting an overvoltage. While reducing the dielectric thickness seems a logical method toward reducing the threshold voltage, the greater current leakage arising from pinholes and other defects[7] in sub-20 nm

films makes this approach impractical for many polymer dielectrics.

Several methods for reducing the overvoltage of thick organic dielectrics rely on using large electric fields to shift V_T closer to zero. Triode-corona charging, borrowed from the electret community, functions as a dielectric preparation technique prior to OSC-deposition. For fully fabricated devices, floating gates and electrostatic prepolarization of the OFET facilitates lower V_T via charge injection into the gate dielectric. Each technique leverages mechanisms ranging from dielectric polarization to direct charge injection, as discussed below.

■ TRIODE-CORONA CHARGING

Corona discharge is a method for charging the surface of an insulating material using a constant high-voltage field. The typical experimental setup for corona discharge relies on a three-electrode setup—or triode—consisting of a bottom plate and top emitting electrode held at a high voltage (∼5−10 kV), and a grid electrode between these two that creates a potential difference between the grid and bottom plate (ca. tens of volts), as shown in Figure 1. This grid ensures that only charges with energy equivalent to the grid potential can strike the bottom plate on which the device substrate is placed. Typical grid potentials for prepolarizing dielectrics range from as low as 15 V to as high as 1000 V, but this voltage must not be so high as to cause dielectric breakdown. The sign of the grid potential is selected to be equivalent to a large top-surface depletion potential: for an n-type (p-type) transistor, the grid potential should be held at a high positive (negative) voltage relative to the grounded bottom electrode.

The long retention times from corona-implanted charging make it an attractive technique for devices requiring long operating lifetimes: the method has been used for decades in the manufacture of electret materials for piezoelectric applications such as microphones and speakers, using methods developed by Sessler and West,[8] and Gross et al.[9] Corona charging has been investigated on hydrophilic polymers such as poly(vinyl alcohol) (PVA);[10] hydrophobic polymers such as polystyrene (PS) derivatives,[11] poly(acrylonitrile-co-butadiene-co-styrene[12] (ABS), and polyethylene[13] (PET); and amphiphobic polymers including Teflon, poly(tetrafluoroethylene) (PTFE),[14] and Cytop.[15,16] Techniques such as thermally
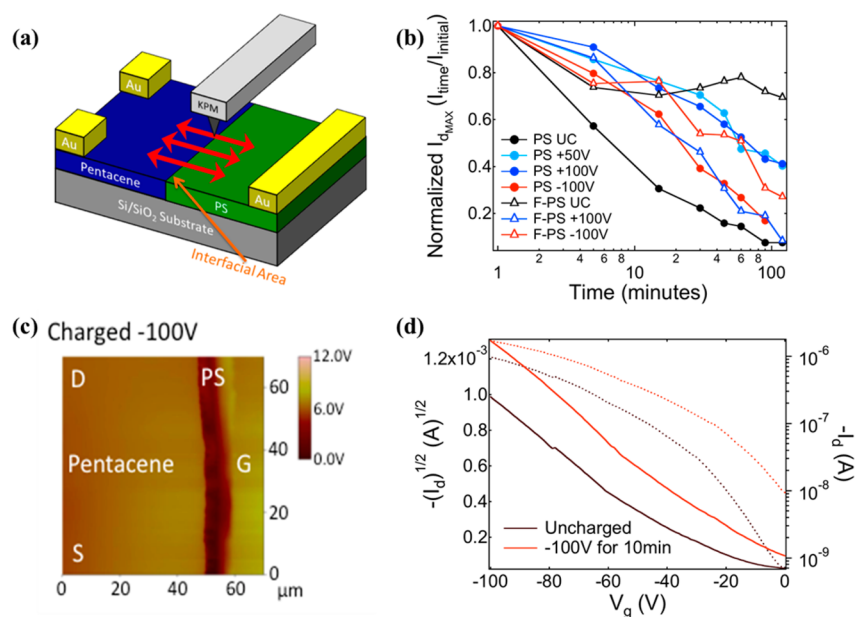
Figure 2. (a) Schematic of a lateral OFET structure in which interfacial potentials can be probed with scanning Kelvin-probe microscopy (SKPM). (b) SKPM surface potential image of lateral OFET, with S, D, and G labeling the Source, Drain, and Gate electrodes, respectively. (c) Decay of the V_T in lateral OFETs with pristine and prepolarized polystyrene (PS) and poly(2-trifluoromethyl styrene) (F-PS) dielectrics. (d) Transfer curves for pristine and prepolarized OFET with a PS dielectric shown in (b), indicating a decrease in the $|V_T|$ toward 0 V. Adapted images reprinted with permission from ref 26. Copyright ACS.

stimulated discharge current (TSDC) have been used to probe the quantity of stored charge and the energy levels where it resides in these dielectrics as a function of temperature.[13] Molinié and others have suggested that the presence of charge injection in the film over polarization is a function of the applied electric field strength.[17] In addition, infrared spectroscopy has been used to identify molecular-level changes of PVDF dielectrics,[18] indicating enhancement of CH_2 rocking modes consistent with an increase in polymer crystallinity.

In our group, Huang et al.[19] performed corona charging in air on a 1 μm thick layer of poly(phenyl-methylsilsesquioxane), a partially cross-linked glass resin. In this study, X-ray photoelectron spectroscopy (XPS) did not identify any changes in chemical composition to suggest ion implantation, and contact-angle characterization of the films before and immediately after charging did not reveal any differences in surface hydrophobicity. Nevertheless, differences in the dielectric's effective surface potential of as much as |45 V| were observed, facilitating controllable threshold voltage shifts of the same magnitude. Our group has also exploited corona charging in a number of device architectures, including dielectric bilayers.[20] Work by Deshmukh et al.[16] utilized a dielectric bilayer of SiO_2 and Cytop, enabling stable charge trapping at the dielectric/dielectric interface. Scharnberg et al. and others have also developed "dual-gate" architectures in which bottom gate/bottom contact pentacene OFETs were encapsulated with a Teflon electret layer that was charged to create a second static gate.[7]

■ PREPOLARIZATION BY GATE STRESSING

Postfabrication approaches for modifying the V_T to enable low-voltage operation have sought to apply the reverse of a gate bias, polarizing the dielectric in a manner that decreases the $|V_G|$ required to switch the transistor. In a method developed by Katz et al.,[21] bottom-gate/top-contact n-type (p-type) OFETs were fabricated with an organic dielectric 1−2 μm thick. After

fabrication, the source and drain electrodes were grounded and the gate was biased to a high negative (positive) voltage in the transistor's depletion regime. This large "charging voltage" is believed to draw minority carriers through the OSC toward the dielectric layer. There, they serve to neutralize majority-carrier traps present at the OSC−dielectric interface, so that subsequent application of V_G results in greater net accumulation of majority carriers at the OSC−dielectric interface that can contribute to I_D. The absolute shifts in the V_T of these devices, ranging up to |60 V|, contribute to the lower V_T. Similar use of a large V_G to prepolarize the dielectric has been applied to OFETs with ferroelectric polymer dielectrics[22,23] and hydrophilic polymers such as PVA.[10,11]

A recent study by Dawidczyk et al.[24] applied scanning Kelvin-probe microscopy (SKPM) to the visualization of charge stored at the OSC−dielectric interface by this gate stressing technique (Figure 2). Fabricated using a previously reported method,[25] layers of ∼50 nm thickness of pentacene and PS were deposited laterally, with two top-contact Au electrodes spaced 250 μm apart and located equidistant from the junction. Application of a large voltage (200 V) between the electrodes resulted in a shift in the surface potential in the PS layer of more than 10 V over an extent of several micrometers into the PS layer, suggesting that these charges are within the dielectric material. In a follow-up investigation,[26] we have fabricated lateral transistors using an analogous pentacene−PS−Au gate stack. Two-dimensional SKPM scans of the transistors revealed a polarization of the entire 3−15 μm lateral span of the organic dielectric. Furthermore, dielectrics consisting of poly(2-trifluoromethyl styrene) exhibited greater V_T stability than PS in the pristine state, while prepolarization enhanced the V_T stability of PS relative to its fluorinated analogue. These data suggest a strong influence of molecular structure and steric effects on charge and/or polarization stability, consistent with previous studies.[18] Moreover, the correlation of greater V_T stability in polymers with HOMO-deepening fluorinated
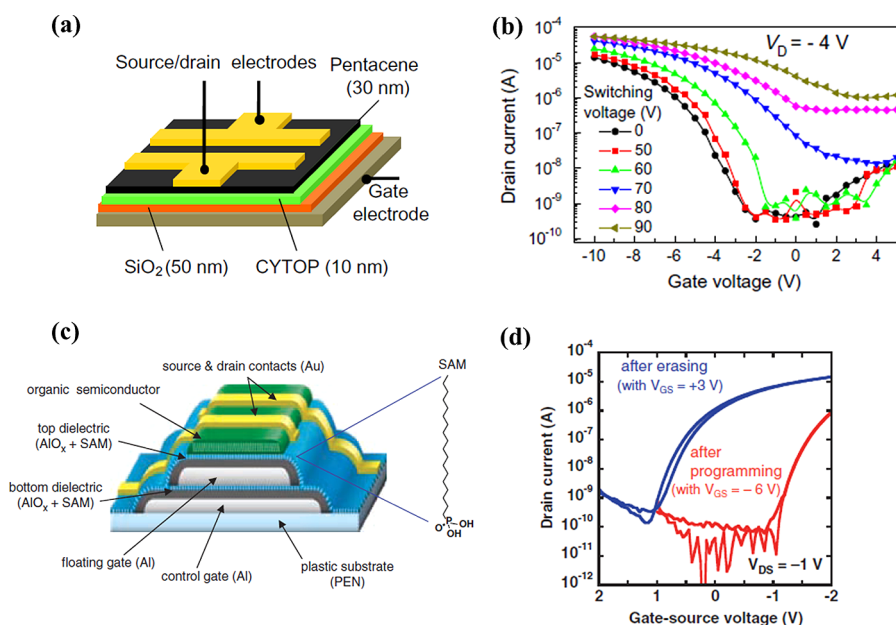
Figure 3. (a) Device diagram of a double-dielectric structure utilizing a CYTOP organic dielectric layer, and (b) transfer characteristics for various writing voltages in a p-channel OFET. Adapted images reprinted with permission from ref 32. Copyright Elsevier. (c) Schematic of a floating gate structure using Al-AlOx for both device and floating gates, and (d) transfer characteristics for a p-channel OFET after programming and erasing steps. Adapted images reprinted with permission from ref 28. Copyright HighWire Press.

species is in agreement with recent theoretical studies of gate bias stress.[27]

FLOATING AND DUAL GATES

Another method that has achieved notable success in manipulating the V_T of OFETs has been the use of floating gates.[28–30] In the floating gate architecture, as shown in Figure 3, an additional metal+dielectric layer is placed in series between the OFET gate dielectric and OSC layers. Upon application of a writing voltage, carriers may be written onto the floating gate layer via thermionic emission or tunneling, where they remain trapped between the floating gate metal and thin encapsulating dielectric. The effect of these trapped carriers on the floating gate is to screen the gate voltage, enabling a shift in the gate voltage required to turn on the OFET. Architectures extended by Chan et al.[31] and Murata et al.[32] employ double- and triple-layer dielectric stacks in a gate stressing scheme to prepolarize an organic dielectric, eliminating the floating gate metal and instead relying on states at the dielectric-dielectric interface for charge storage and V_T modification.

SELF-ASSEMBLED MONOLAYERS

As discussed previously, there are often significant constraints on the materials, processing parameters, and dimensions of dielectrics used in OFETs. In many cases, the best solution may be to modify an existing dielectric surface to make OFET operation viable. An area of active research for dielectric enhancement is the use of self-assembled monolayers (SAMs). Although not a strict classification, SAMs are molecules that (a) form a covalent bond with a surface (in contrast to most Langmuir−Blodgett films) and (b) form an ordered single layer of molecules on said surface. It is important to note here that while grafted oligomers and brush polymers have also been used extensively to modify polymer and inorganic surfaces, they

generally do not make well-ordered molecular layers, and as such fall outside the scope of this Account.

The processes used to adsorb SAMs on a surface should yield densely packed, well-ordered layers, although OFETs with a glasslike organization of SAM headgroups has been reported.[33] The low molecular weight of most SAMs allows them to be deposited from either a vapor or solvent solution. For both processes, postattachment annealing promotes layer crystallinity and structural stability at high postprocessing temperatures[34] required for device fabrication. A notable method developed by the Bao group yields very smooth crystalline SAMs upon annealing in ammonia vapor.[35]

The simple processing requirements for SAM modification of dielectrics have stimulated the development of a wide array of complementary dielectric-SAM systems that can be employed in OFETs. There are now a number of commercially available SAM molecules with reactive anchor groups compatible with attachment to the surface oxides of the most commonly used inorganic dielectrics, as shown in Table 1. In addition, a

Table 1. Some of the Most Commonly Used Oxide Dielectrics and Compatible SAM Anchor Groups

SAM/reactive group	surface
$-SiCl_3$, $-Si(OCH_3)_3$, $Si(OC_2H_5)_3$	SiO_2
$-CO(OH)$	SiO_2, Al_2O_3 ITO, ZTO
$-PO(OH)_2$, SANDs[a]	SiO_2, Al_2O_3, ZrO_2, TiO_2, HfO_2

[a]For an illustration of SAND layers see Figure 4.

number of groups have designed platforms that enable the construction of multilayer SAMs. Among these, the Marks group has developed self-assembled nanodielectrics (SANDs),[36] which exploit a type of reaction pioneered by Katz et al.[37] to build multilayer molecular dielectrics interconnected with metal oxide groups including SiO_2, Al_2O_3, ZrO_2, and HfO_2 groups. For a detailed description of

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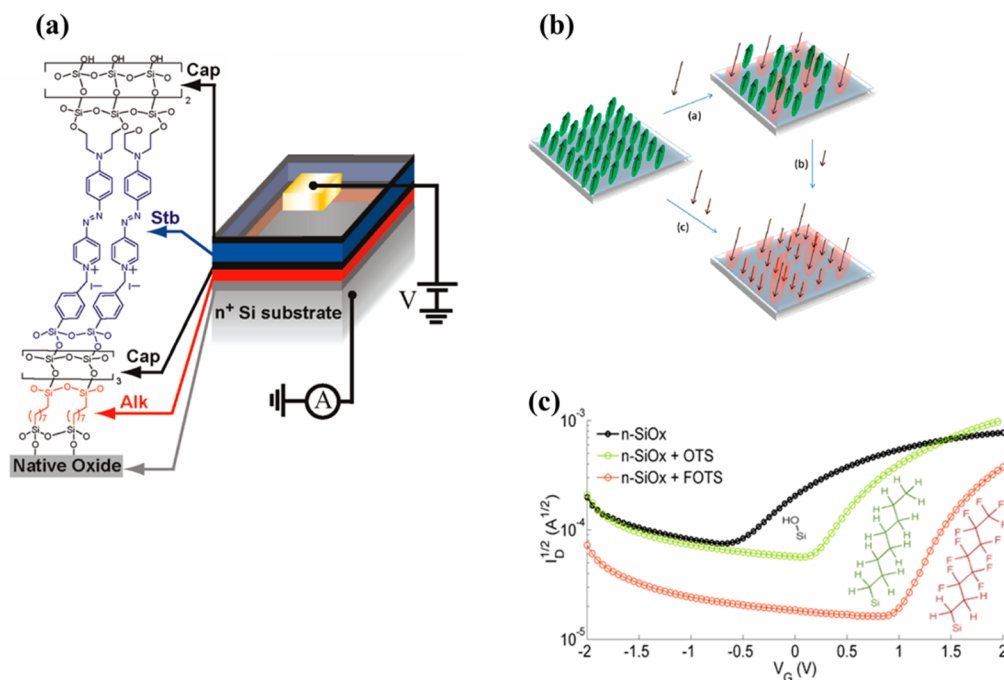dx.doi.org/10.1021/ar5000049 | Acc. Chem. Res. 2014, 47, 1369−1377

Figure 4. (a) Metal−insulator-semiconductor structure utilizing a self-assembled nanodielectric (SAND) consisting of alkyl and stilbazolium interlayers. Adapted image reprinted with permission from ref 59. Copyright 2010 American Chemical Society. (b) Schematic illustrating the tunability of a substrate surface potential with mixed monolayers of opposite dipoles. Adapted image reprinted with permission from reference 42. Copyright 2010 American Chemical Society. (c) Application of monolayers of OTS and FOTS to a nanoscale silicon oxide shifts V_T with increasing dipole magnitude, and results in a decrease of the subthreshold leakage for FOTS. Adapted image reprinted with permission from ref 60. Copyright 2013 American Chemical Society.

the chemistry and materials selection criteria for SANDs, we refer the reader to a recent Account on the subject.[38]

The interdependence of device properties like mobility and V_T on the surface energy and molecular disorder at the OSC−dielectric interface is well documented.[39] A recent investigation by Chung et al. examined the bond dipole difference between chemically similar octylphosphonic acid and octyltriethoxysilane SAMs, effectively decoupling the influence of OSC morphology on the electronic properties of the fabricated OFETs.[40] Moreover, properties of the SAM that influence V_T, such as the monolayer polarizability, depend on the cooperative interactions between individual molecules.[41,42] This observation has stimulated the investigation of the properties of mixed monolayers as a way to tune V_T controllably.[43−46] Recently, the Klauk group has demonstrated nearly continuous tuning of the threshold voltage in OFETs employing varying surface concentration ratios of octadecylphosphonic acid and its fluorinated counterpart.[47]

The use of dipolar SAMs to shift the V_T, as well as the nature of this V_T shift, has been the focus of numerous investigations.[48−51] To ascertain whether the SAM dipole induces charge in the OSC, Podzorov and co-workers have used electron spin resonance (ESR) to identify signatures of free electrons in single-crystal rubrene treated with FTS.[52] This V_T shift has been associated with a Helmholtz potential, V_{SAM}, that arises from the intrinsic dipole of the constituent molecule.[53] The Halik group recently investigated the role of this intrinsic dipole on the V_T shift for a broad range of dipolar SAMs and n- and p-type OSCs, and observed a linear relationship between the dipole moment and the shifted V_T.[54] de Leeuw's group has demonstrated that a change in the trap density at the OSC-dielectric interface resulting from SAM modification is responsible for the observed V_T shift in

OFETs.[55] The potential V_{SAM} has been measured using scanning Kelvin-probe microscopy,[56] and recently the Österbacka group and our own have applied charge extraction in a linearly increasing voltage (CELIV) to measure V_{SAM} on native alumina.[57]

Our group has exploited the polarity of commercially available silanes to tune the V_T of OFETs.[58] Huang fabricated p-channel OFETs of 5,5′-bis(4-hexylphenyl)-2,2′-bithiophene (6PTTP6) on SAM-treated 300 nm thick SiO_2, and observed V_T shifts as small as −5 V for the nonpolar phenyltrimethoxysilane (PTS) and as high as +80 V for the dipolar perfluorodecyltrichlorosilane (FDTS). Leveraging the large V_T difference between the two SAM-treated OFETs enabled operation of unipolar inverters with a switching voltage of −20 to 30 V and gains as high as 7, as an approach to single-OSC digital logic.

In addition to modifying the V_T, our group has sought to address gate leakage, the unwanted current flow from gate to source or drain that contributes to a circuit's power consumption. We recently demonstrated the use of dipolar SAMs of octyl- (OTS) and perfluorooctyltriethoxy silane (FOTS) as electrostatic barriers for reducing leakage in n-channel OFETs fabricated on a marginal quality 10 nm SiO_2 dielectric.[60] Both SAMs were shown to reduce gate leakage by an order of magnitude, as compared to OFETs fabricated on bare oxide (Figure 4). Most notably, comparison of OFF currents revealed that FOTS reduced subthreshold leakage by more than 3 orders of magnitude, while OTS only reduced it by an order of magnitude. In addition, the switching efficiency of the transistors was greatly increased by SAM modification. Analysis of this switching behavior indicated an increase in the trap density at the OSC−dielectric interface, consistent with recent reports by de Leeuw et al.[55] The reduction of

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subthreshold leakage with increasing molecular dipole, coupled with V_T shifts that follow the same trend, opens up new possibilities for the use of SAMs as interfacial tuning agents.

As discussed above, the threshold voltage can be influenced by parameters such as morphology and interface traps at the OSC−dielectric interface. Another interface that can influence the operating voltage of an OFET is that between the active layer OSC and the Source/Drain electrodes, the site of the contact resistance R_C. An increase in the R_C causes the requirement of a higher circuit driving voltage V_{DD} to ensure proper switching at subsequent circuit stages, and consequently also increases the power consumption of the circuit. When the materials at this interface have the same compositions and morphologies as the bulk regions of those materials, then the physical origin of the contact resistance[61,62] is an energy offset between the Fermi level of the electrode metal and the highest-occupied molecular orbital (HOMO) or the lowest-unoccupied molecular orbital (LUMO) of the OSC. This resulting voltage barrier is related to the change in work function of the electrode metal when an OSC is deposited thereon. On the other hand, when the OSC composition or morphology is different near the electrode interface, then the R_C element can be modeled as an OFET in its own right, in series with the main channel, and having its own mobility and V_T.[63]

Several groups have employed SAMs to modify the contact resistance of p-channel OFETs in both bottom-gate/bottom-contact and top-gate/bottom-contact geometries.[64,65] In particular, the aforementioned chemical selectivity of SAM anchor groups enables controlled modification of source/drain electrodes without modifying the dielectric surface.[66] Our group has extended use of this SAM toolbox to n-channel NTCDI OFETs,[67] assessing the effect of both SAM-modified dielectrics and Au electrodes. Bottom-contact OFETs using electrodes treated with perfluorooctylthiols resulted in performance similar to top-contact OFETs, which typically exhibit superior performance.[68] de Leeuw and co-workers have used OFET structures to investigate Au electrodes treated with perfluorodecane- and perfluorohexadecanethiol SAMs, assessing their relative impact on morphology and contact resistance[69] In that work, it was demonstrated that the tunneling barrier seen by carriers traversing the SAM at the Au electrode was responsible for the increased contact resistance observed in OFETs with SAM-treated electrodes. A comparable method for treating electrodes to tune their work functions combines the advantages of polymer processing with the thin polarizable layers associated with SAMs. This method developed by Kippelen and co-workers exploits the degree of protonation in ultrathin aliphatic amine polymers spin-cast from different pH solutions to effect work function changes tunable by more than 1 eV.[70] Notably, this method overcomes the limitations of surface-specific binding required for SAM-treatment of electrodes, enabling the use of electrode materials inaccessible to direct SAM chemisorption. It is relevant to mention that while SAM site-specific binding may appear to limit their incorporation in devices with organic substrates, a successful chemical approach for SAM treatment of a poly(ethylene terephthalate) (PET) surface has been demonstrated by Xiang and co-workers[71] by creation of a polysiloxane layer onto which silane SAMs could chemisorb.

■ CHALLENGES AHEAD AND OUTLOOK

Although each of these methods offers unique ways to modify device properties, their viability beyond the laboratory in large-scale, high-throughput fabrication of OSC-based electronics must also be considered. The corona method has enabled mass-production of electrets for audio applications, but integration with circuit fabrication presents a few challenges. First, because corona charging is routinely done in an air environment, its effectiveness is highly dependent on relative humidity[72] and charging temperature,[73] placing restrictions on postcharging fabrication processes. In addition, the corona itself only extends a few millimeters radially from the top point electrode. To address this particular issue, our group has demonstrated a direct-write technique for implanting charge using a low energy electron beam,[16] analogous to corona charging. However, this writing procedure is by nature a serial process, and will require additional engineering to meet the needs of high-throughput fabrication methods.

Gate stressing, by comparison, has the advantage that the method is independent of any particular fabrication technique, and could be applied using high-throughput stamping. The challenges associated with its full-scale implementation center on circuit design, as the writing of the V_T demands additional logic stages that can access a high driving voltage V_{DD} to write to the OFET gate. This arrangement is suitable in organic memories,[21] but still relies on complementary gates with stable V_T. Fabrication of multistage logic blocks that leverage the addressability of field-programmable gate arrays (FPGAs) could make this technique viable for high-sensitivity analyte sensors.

SAMs may offer the most practical solution for writing the V_T of many gates simultaneously. Zhu and co-workers have employed spiropyran SAMs with light-switchable dipoles that enable optical control over the threshold voltage,[74] making possible large-scale optical memories. Fabrication methods that integrate the ability to tune both n- and p-channel OFETs with adsorption of a single dipolar SAM moiety will come at the cost of additional processing steps. Fortunately, the development of low temperature solution processes may enable roll-to-roll processes in which SAM modification entails only marginal addition of processing equipment. Additionally, the broad materials palette available to newly developed polymer-based methods for modifying device electrodes may prove even better candidates for integration with organic and hybrid electronic device fabrication.

Ultimately, refining our understanding of the physical mechanisms that underlie each of these methods will allow us to harness their full potential for independently tuning the V_T, mobility, and leakage currents in OFETs, and direct us toward the clearest path to bringing OFET-based electronics into practical usage.

■ AUTHOR INFORMATION

Notes

The authors declare no competing financial interest.

Biographies

Josué F. Martínez Hardigree received a B.Sc. from Massachusetts Institute of Technology (MIT) in 2007, in Materials Science and Engineering with a focus on electronic materials. Before undertaking his Ph.D. at Johns Hopkins University (JHU) as an NSF Graduate Research Fellow, he worked as an investment analyst for the MIT Investment Management Company. Presently, he is focused on understanding charge trapping at interfaces in organic field-effect transistors.

Howard E. Katz is currently Chair of the Department of Materials Science and Engineering at JHU. He received his B.Sc. from MIT in 1978 and his Ph.D. from UCLA in 1982. He was a Member of Technical Staff at Bell Laboratories from then until 2004, and promoted to Distinguished Member of Technical Staff in 1998. He is a fellow of the American Chemical Society, American Physical Society, Materials Research Society (MRS), and the American Association for the Advancement of Science, and was MRS President in 2004.

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